Attorney Docket No. 5308-279 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Sei-Hyung Ryu
Serial No.: 10/698,170
Filed: October 30, 2003
For: **VERTICAL JFET LIMITED SILICON CARBIDE POWER METAL-OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTORS**

Group Art Unit: 2818
Confirmation No. 2502
Examiner: Long K. Tran

DECLARATION OF MR. SEI-HYUNG RYU PURSUANT TO 37 C.F.R. 1.131

Sir:

I, Sei-Hyung Ryu, hereby declare and say that:

1. I am the inventor of the subject matter of the rejected claims.

2. Prior to December 18, 2002, I conceived the invention claimed in the rejected claims.

3. In support of the above statement of Section 2, I hereby submit as **Appendix A** a copy of an invention disclosure I prepared and submitted to the Cree, Inc. patent department before December 18, 2002 showing conception of the claimed invention. The dates within this document have been blocked out, but are before December 18, 2002.

4. Due diligence was exercised from prior to December 18, 2002 to the filing of the present patent application.

5. In support of the above statements of Section 4, I hereby submit as **Appendix B** a copy of a letter dated December 16, 2002, requesting that Myers Bigel Sibley and Sajovec, P.A. prepare an application relating to "*A Novel Planar Power MOSFET Transistor in Silicon Carbide with Vertical JFET Limiter to Reduced JFET Resistance and a Method of Fabrication*"; as **Appendix C** a copy of a letter from Myers Bigel Sibley & Sajovec, P.A. dated December 19, 2002, forwarding an initial draft of a patent application for inventor review; and as **Appendix D** a copy of a letter dated December 20, 2002, stating that the draft

application was filed on December 20, 2002 as a provisional application (U.S. Application No. 60/435,212). The present application claims the benefit of priority from this provisional application.

6. In summary, my statements herein and the documents I have concurrently submitted show conception of the invention prior to December 18, 2002 coupled with due diligence from prior to December 18, 2002 to the filing of the priority provisional application on December 20, 2002.

7. I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true. I further declare that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Sei-Hyung Ryu 7/25/2006.

Sei-Hyung Ryu Date

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Filing Recommendation	For IP Committee Use
IP Committee Review Date:	Disclosure Number: 1D6236
Committee Recommendation: ☒ File Disclosure Complete ☐ File Prepare Full Disclosure ☐ Do Not File ☐ Publish Without Filing ☐ Review Further ☐ Keep as Trade Secret	Date Opened: [redacted]
Comments:	

Invention Disclosure

To: Associate General Counsel for Intellectual Property

1. *Invention Title: A novel planar power MOSFET transistor in silicon carbide with vertical JFET limiter to reduced JFET resistance, and a method of fabrication*

2. Inventors:

	Inventor No. 1	Inventor No. 2	Inventor No. 3
Full name	Sei-Hyung Ryu		
Home Address	123 Louben Valley Court Cary, NC 27513		
Work Phone	919-313-5541		
Citizenship	Korea		
Department	Powe R&D		
Manager	Anant Agarwal		
Wrote Disclosure	☒ Yes ☐ No	☐ Yes ☐ No	☐ Yes ☐ No

Attach additional sheets if necessary

3. Date invention conceived: _____ Date invention reduced to practice: _____

4. Invention developed under government contract? Yes ☑ No ☐ Internal Contract No.: 1095

IMPORTANT: If you have any question as to whether the invention was developed (i.e. conceived or first reduced to practice) under a government contract, please contact the contract manager.

5. Identify any disclosures of the invention outside the company. For example, identify any publication, abstract, offer for sale or sale, discussions with suppliers or customers, etc., in which the invention was described. Give the date and place of any such disclosures. (attach additional sheets if necessary): Darpa review, _____

6. Identify any anticipated disclosures of the invention outside the company.: _____

7. Identify any related inventions or disclosures by Cree personnel: _____

8. Identify products in which the invention may be used: please see attached paper

Remember to have each page of your invention disclosure signed and dated by a witness.

Please attach this cover form to your invention disclosure, along with any relevant documentation. Submit the disclosure to David Hall, Silicon Drive x5343.

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) Sei-Hyung Ryu		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

A B

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Description of Invention

Answer each of the following questions about your invention. Use additional space or attach additional sheets as necessary. Attach copies of notes, diagrams, lab notebooks, journal articles, etc. if available. Have a witness sign and date each sheet of the disclosure, including additional sheets.

1. Provide a brief description of the invention. What problem does it solve, and how does it solve the problem?

please see attached paper

2. How does the invention differ from present technology? What are the novel or unusual features of the invention? What advantages does it possess?

please see attached paper

3. Describe specific embodiments or examples of the invention, if any. Does the invention have any alternative embodiments? Enclose sketches, drawings, photographs and other materials that help illustrate the description.

please see attached paper

4. What are possible applications for the invention? In addition to immediate applications, are there other uses that might be feasible in the future?

please see attached paper

5. List any documents or publications which relate to important aspects of this invention.

please see attached paper

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1)		(1)	
(2)		(2)	
(3)		(3)	

A novel planar power MOSFET transistor in silicon carbide with vertical JFET limiter to reduced JFET resistance, and a method of fabrication

Brief Description

Double implanted MOSFET structure is one of the most promising structures in silicon carbide because it provides a combination of a reasonable gate packing density and a good protection of its MOS gate regions. However, the on-resistance of a conventional DMOSFET with structure shown in Figure 1. is severely limited due to the JFET resistance and uneven current flow, especially in 6H-SiC. It has been suggested that introducing a spacer implantation in between the p-well regions alleviates this problem (V. R. Vathulya, H. Shang, M. H. White, *IEEE Electron Device Letters*, Vol. 20, No. 7, p.354 July 1997). However, the JFET region in DMOSFET structure can extend deep into the drift layer, effectively make the JFET channel length much longer than the P-well junction depth, as shown in Figure 1. The JFET implant region presented by Vathulya can be only as deep as the p-well regions because the implant energy is limited. Therefore, that method does not significantly reduce the JFET resistance if the depletion region formed at the p-well and the n- drift layer interface extends deep into the n- drift layer.

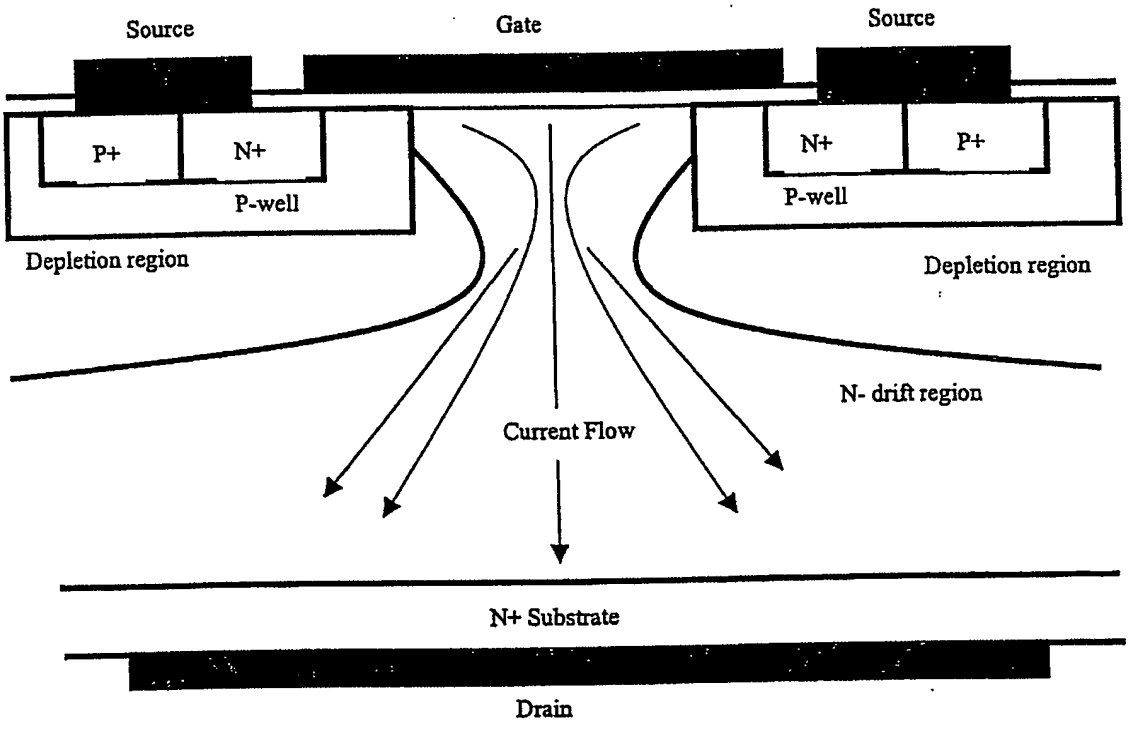

Figure 1. Conventional DiMOS structure

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
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(3)		(3)	

The DiMOS structure suggested in this invention reduces the JFET resistance using an additional n-doped epilayer with slightly higher doping concentration. This epilayer provides higher doped regions between the p-wells as well as a higher doped regions underneath the p-well regions. The depletion width in the JFET region is reduced due to higher doping level in the N region, and therefore, the channel length of the built-in vertical JFET is dramatically reduced. Similar structure was used in UMOSFETs in SiC (J. Tan, J. A. Cooper, Jr., and M. R. Melloch, *IEEE Electron Device Letters*, Vol. 19, p. 487, 1998), however, structure shown in this paper has implanted p-layers under the trenches which create more JFET resistance. This structure helps reducing the total on-resistance without sacrificing the blocking voltage which is shown by a 2D numerical simulation (Fig.2 –7). The simulations are done for devices capable of withstanding 10000V at blocking state. The experimental results (Fig. 8-9) show that the new structure results in approximately 30% lower on-resistance compared to conventional structure.

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1)		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

Assumtions for simulations:

115 μm thick, $6x10^{14}$ cm^{-3} doped n-type epilayer used as drift layer

Bulk electron mobility = 600 cm^2/Vs

MOS mobility = 20 cm^2/Vs

t_{ox} = 500 Å

Gate Length = 1.5 μm

Cell pitch = JFET gap + 20 μm

On-resistance measured at V_{GS} = 12 V (V_g-V_t = ~ 8.5 V)

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) [signature]		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

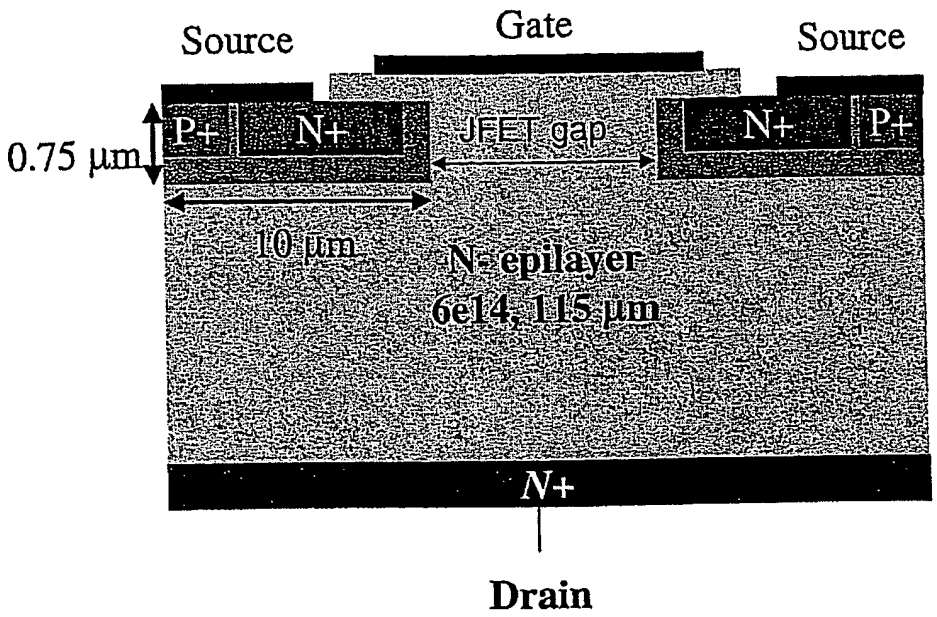

Fig. 2 simulation structure

Effect of JFET gap on 10 kV device performance

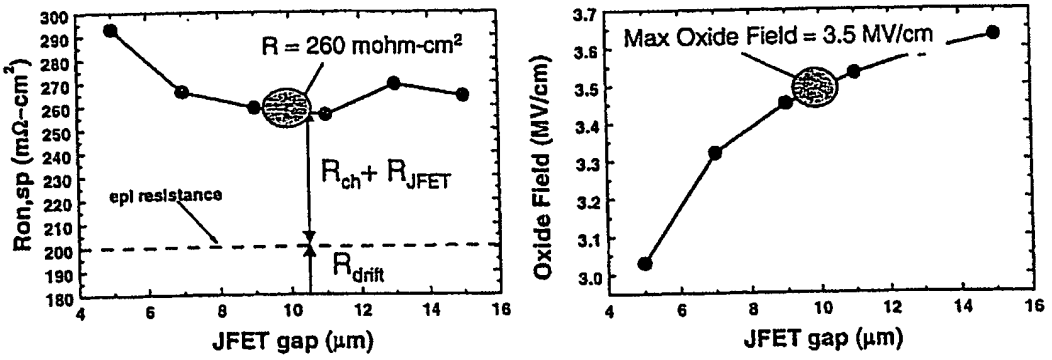

Figure 3. Simulation results for conventional structure

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) Siyoung Mo		(1) Arvind Agarwal	
(2)		(2)	
(3)		(3)	

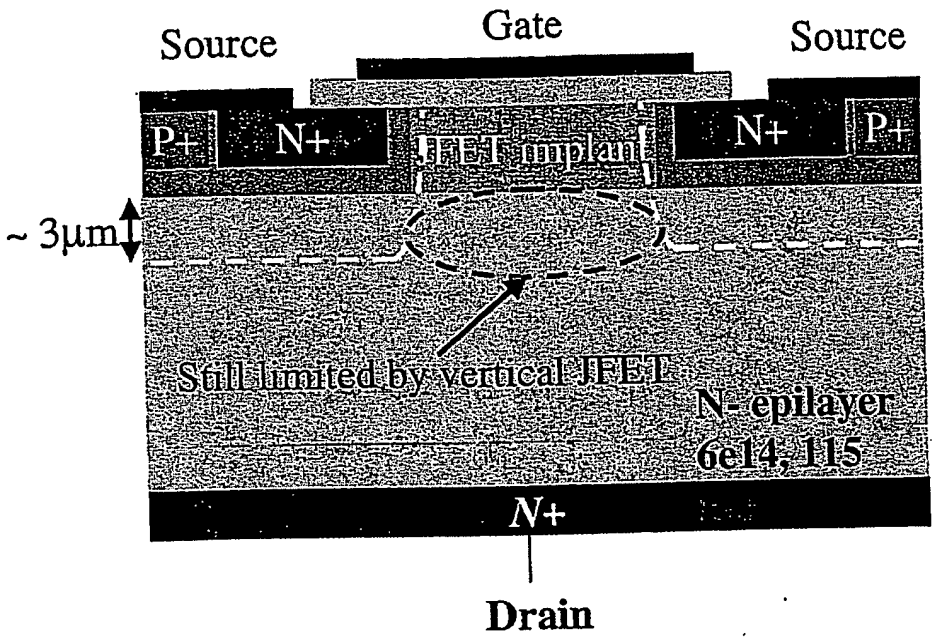

Figure 4. Structure with JFET implant only (Vathulya et al.)

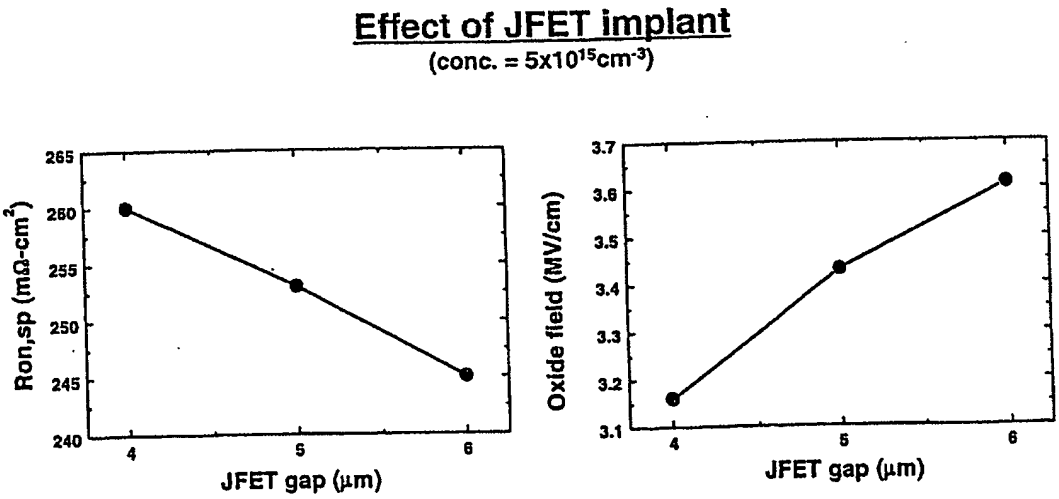

Figure 5. Simulation results for conventional structure with JFET implant only

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) Sei-Hyung Ryu		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

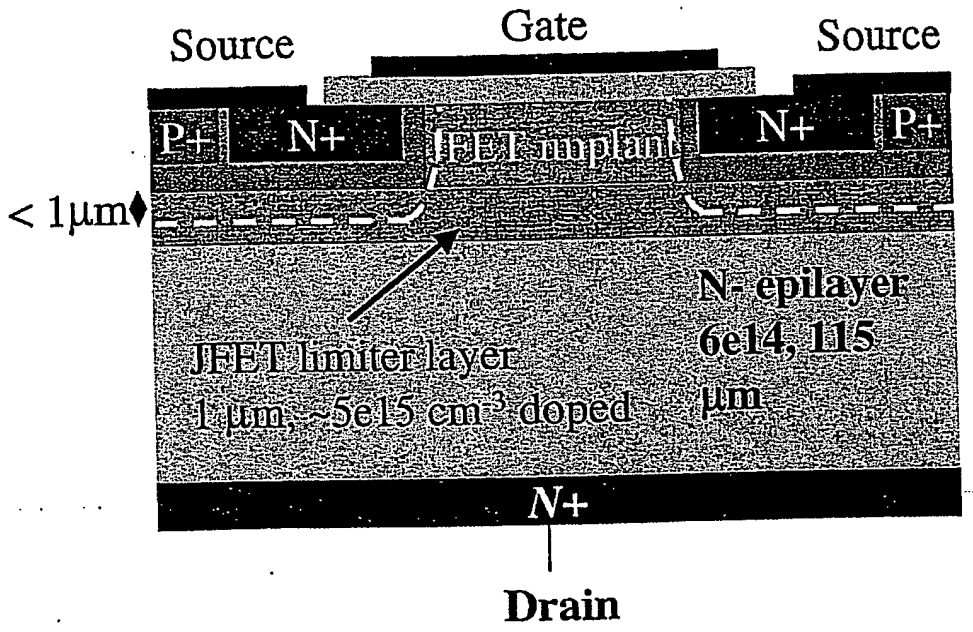

Figure 6. Structure with JFET limiter layer – this invention

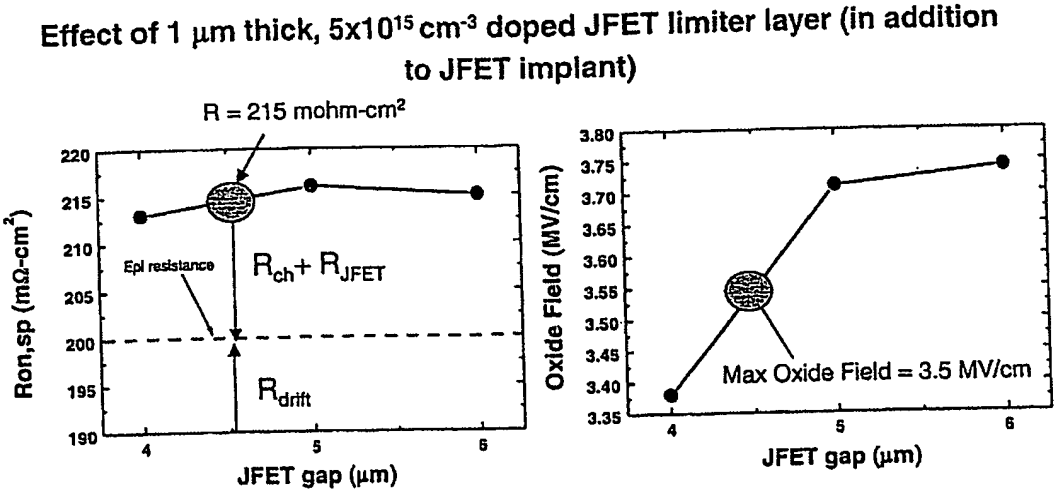

Figure 7. Simulation results for DMOSFET structure with JFET limiter (this invention)

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
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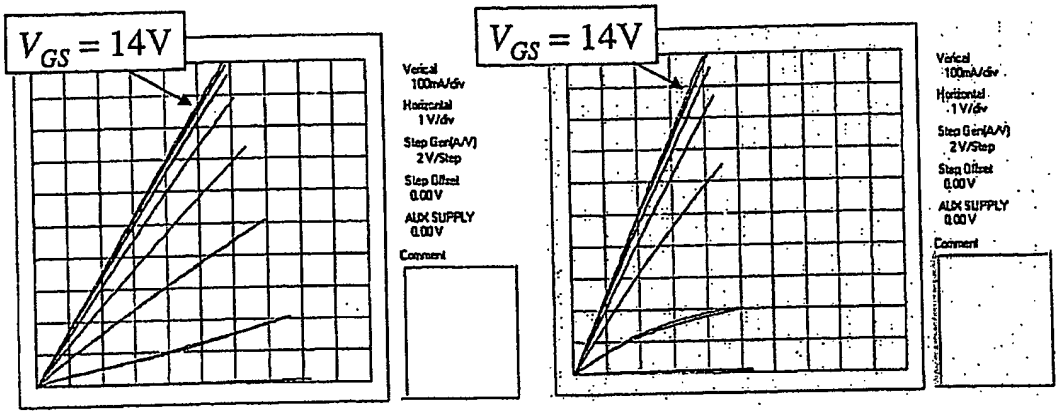
(3)		(3)	

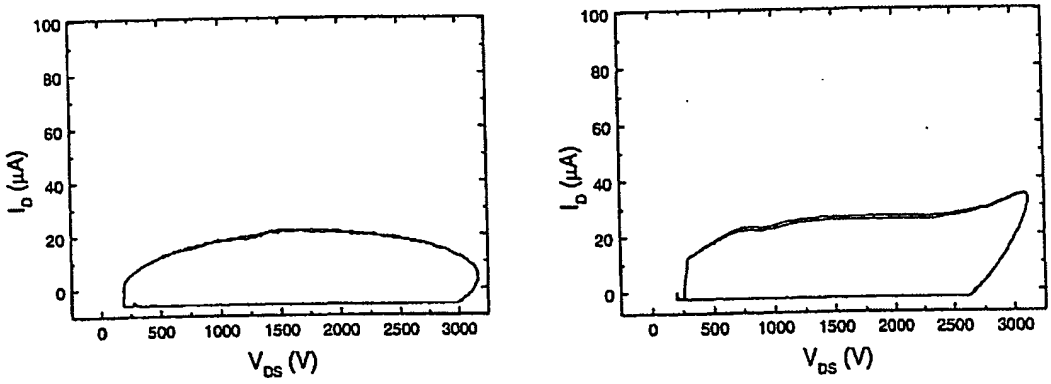


DMOSFET *without* JFET limiter
266 mΩ-cm^2

DMOSFET *with* JFET limiter
189 mΩ-cm^2

Figure 8. Experimental results for DMOSFET structure with and without JFET limiter –on-state

Measurement limited by equipment - Tektronix 371A



DMOSFET *without* JFET limiter
(V_{GS} = -4V)

DMOSFET *with* JFET limiter
(V_{GS} = -5V)

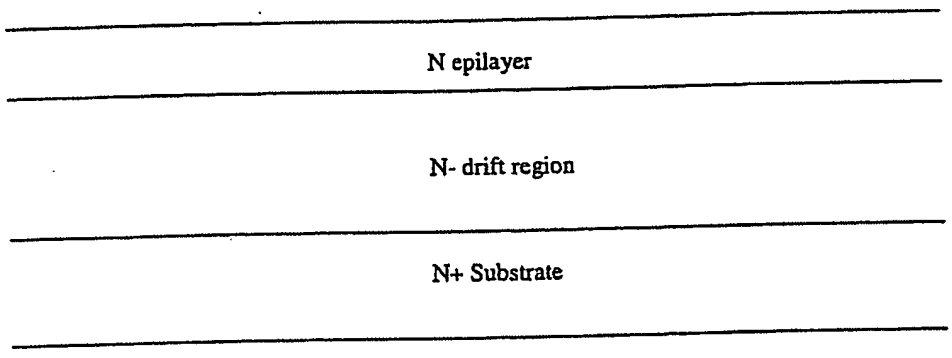
Figure 9. Experimental results for DMOSFET structure with and without JFET limiter –off-state

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) Sei-Hyung Ryu		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

Method of fabrication

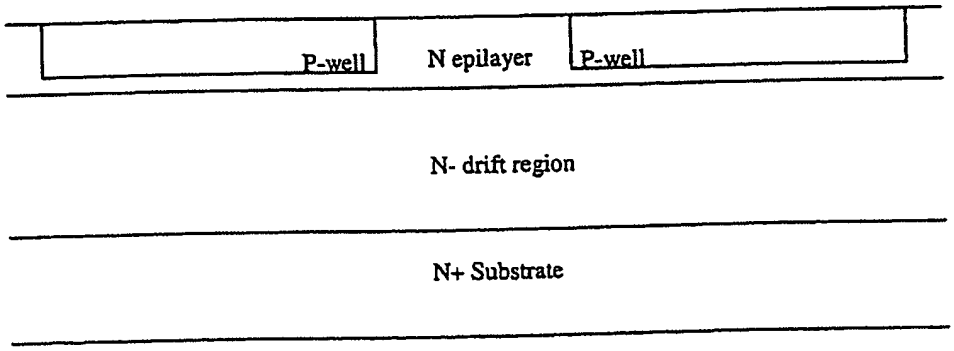
1. Epi structure

Fabrication process begins with the epi structure shown below. A lightly doped N- drift region is grown in a N+ substrate. The doping of the N- drift region should range from $1e14cm^{-3}$ to $5e16cm^{-3}$, and the thickness should range from 5μm to 150μm. N-type epilayer is then grown on top of N- drift layer. The doping of this layer should range from $1e15cm^{-3}$ to $5e17cm^{-3}$, and the thickness should be 0.5μm to 1.5μm.



2. P-well Implantation

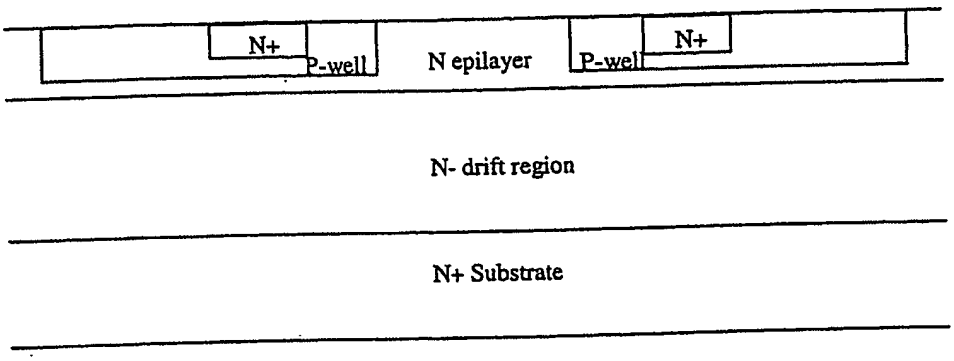
P-well is formed by ion implantation. P-type species, such as Boron or Aluminum should be used for this implantation. The junction depth should be from 0.3μm to 1.2μm, which must be shallower than the thickness of the N epilayer. The concentration of this well should range from $1e16cm^{-3}$ to $1e19cm^{-3}$. The doping profile of the p-well can be a box profile, a retrograde profile (heavier concentration at the bottom of the p-well, lighter concentration at the top of the p-well), or totally buried (with some n-type layer on top of the p-well).



Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) Seq. Hyung Kim		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

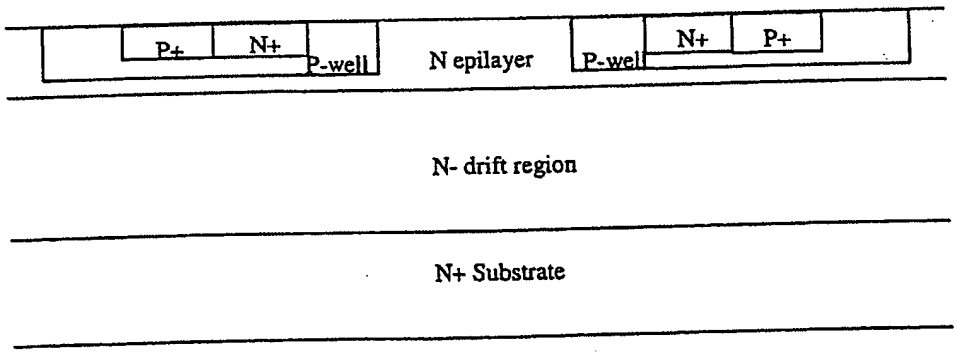
3. Source Implantation

N+ Source regions are formed by ion implantation. N-type dopants, such as phosphorus and nitrogen can be used. The doping concentration should range from $5e18cm^{-3}$ to $1e21cm^{-3}$, and the depth of these regions, which must be shallower than that of the P-well, should be 0.1μm to 0.8μm.



4. P+ contact implantation

For better p-type ohmic contacts, p+ regions are formed using ion implantation. P-type dopants, such as Aluminum, Boron should be used. The doping of this region should be $5e18cm^{-3}$ to $1e21cm^{-3}$, and the depth should be 0.2μm to 1.2μm, which must be shallower than that of the p-well.



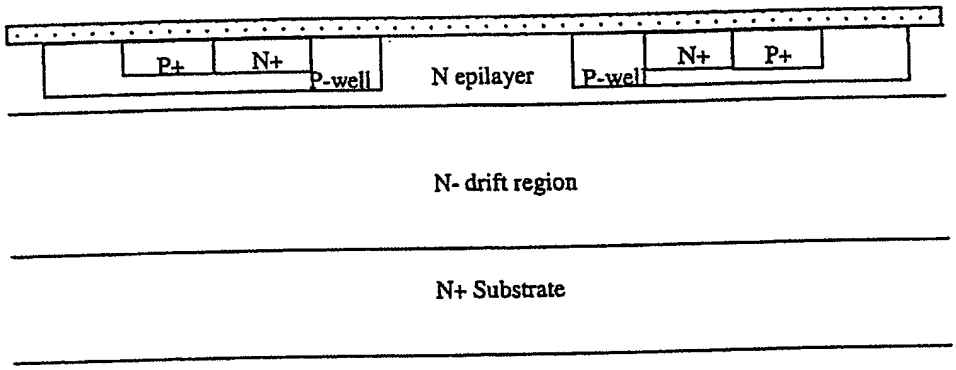
Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) Ser Hyeong Ryu		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

5. Implant activation

All implants are activated in a suitable ambient at temperatures ranging from 1200 °C to 1800 °C. Duration of this activation is from 30 seconds to 24 hours. The surface of the wafer can be capped with a dielectric layer such as SiO_2 or Si_3N_4 to protect the wafer surface during anneal.

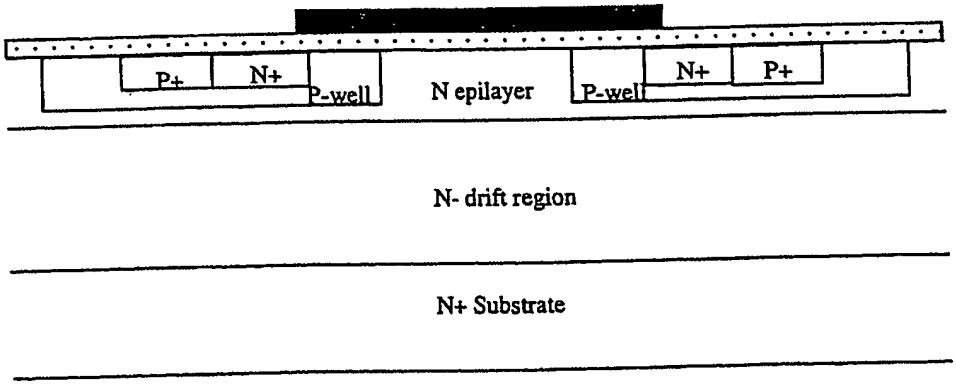
6. Gate dielectric formation

After the implant activation, a suitable gate dielectric material is deposited or grown on top of the structure.



7. Gate metal deposition

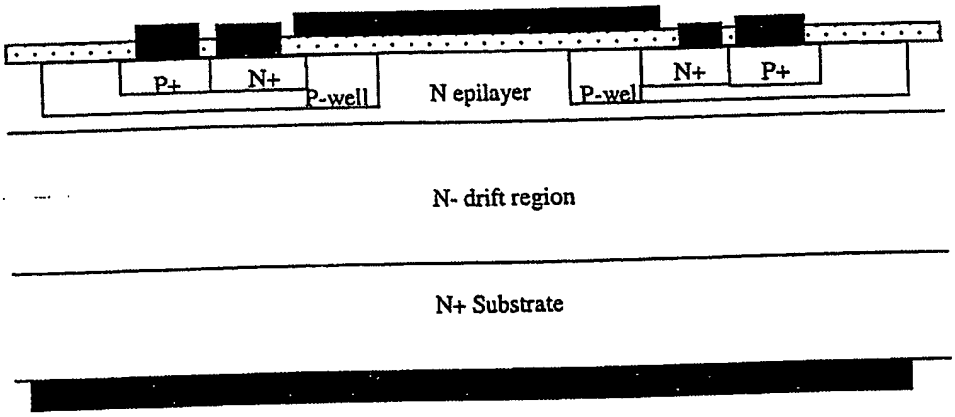
Gate metal is deposited then patterned to form gate electrodes. Metals such as Molybdenum or polysilicon can be used at this step.



Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) Jeff Hyung Ryu		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

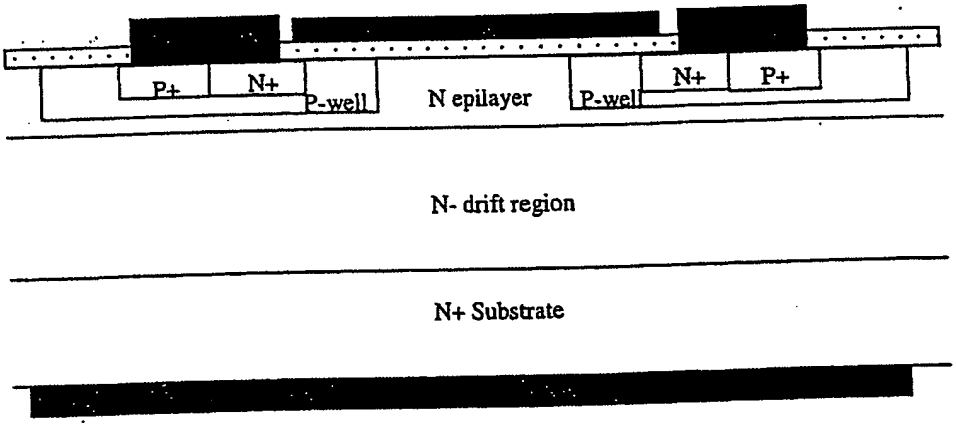
8. Formation of Contacts

Contact windows are open in the dielectric layer and contact metal is deposited. Ni or Ti is typically used for N-type ohmic contacts and Ni, Ti, Pt, or Al is used for P-type ohmic contacts. After the metal deposition, the contacts are sintered in vacuum or in Argon at temperatures from 500°C to 1200°C, for a duration ranging from 1 sec to 20 minutes.



9. Overlayer

Finally, overlayer metal is deposited and the fabrication is complete.

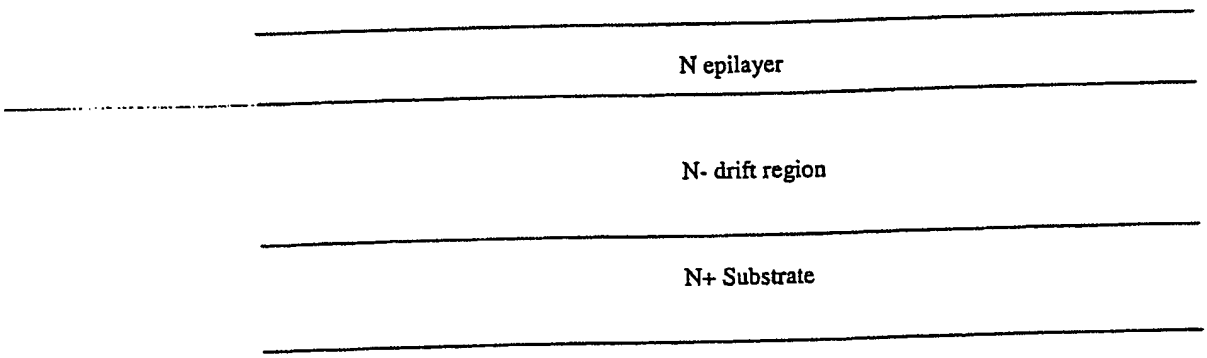


Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1)		(1) Arant Agarwal	
(2)		(2)	
(3)		(3)	

Alternative method

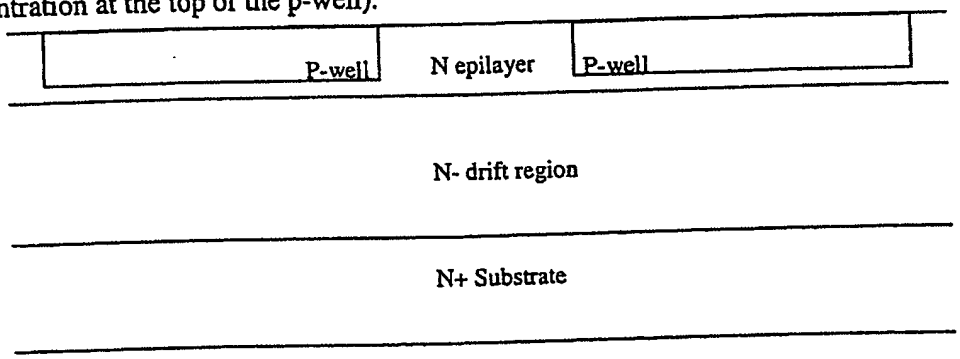
1. Epi structure

Fabrication process begins with the epi structure shown below. A lightly doped N- drift region is grown in a N+ substrate. The doping of the N- drift region should range from 1e14cm^{-3} to 5e16cm^{-3}, and the thickness should range from 5μm to 150μm. N-type epilayer is then grown on top of N- drift layer. The doping of this layer should range from 1e15cm^{-3} to 5e17cm^{-3}, and the thickness should be 0.5μm to 1.5μm.



2. P-well Implantation

P-well is formed by ion implantation. P-type species, such as Boron or Aluminum should be used for this implantation. The junction depth should be from 0.3μm to 1.2μm, which must be shallower than the thickness of the N epilayer. The concentration of this well should range from 1e16cm^{-3} to 1e19cm^{-3}. The doping profile of the p-well can be a box profile, or a retrograde profile (heavier concentration at the bottom of the p-well, lighter concentration at the top of the p-well).



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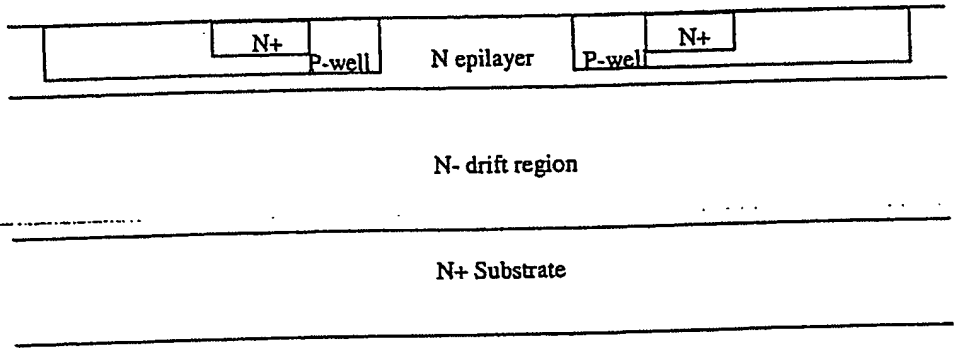
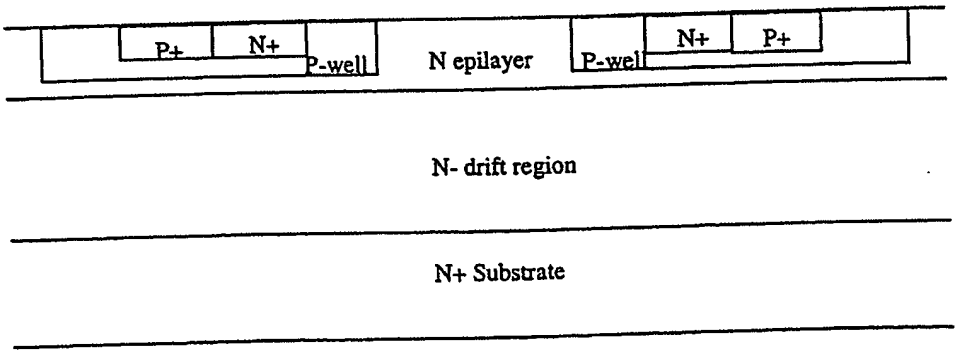
3. Source Implantation

N+ Source regions are formed by ion implantation. N-type dopants, such as phosphorus and nitrogen can be used. The doping concentration should range from $5e18cm^{-3}$ to $1e21cm^{-3}$, and the depth of these regions, which must be shallower than that of the P-well, should be 0.1μm to 0.8μm.



4. P+ contact implantation

For better p-type ohmic contacts, p+ regions are formed using ion implantation. P-type dopants, such as Aluminum, Boron should be used. The doping of this region should be $5e18cm^{-3}$ to $1e21cm^{-3}$, and the depth should be 0.2μm to 1.2μm, which must be shallower than that of the p-well.



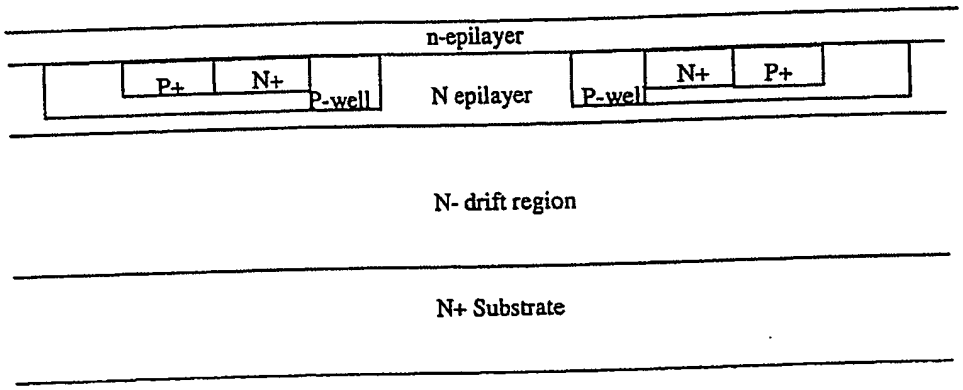
Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) Jer-Tyang Chen		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

5. Implant activation

All implants are activated in a suitable ambient at temperatures ranging from 1200 °C to 1800 °C. Duration of this activation is from 30 seconds to 24 hours. The surface of the wafer can be capped with a dielectric layer such as SiO_2 or Si_3N_4 to protect the wafer surface during anneal.

6. Epi regrowth

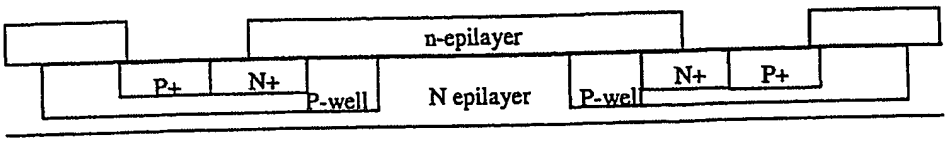
A thin n-type epilayer is grown on top of the structure to form channel region. The doping of this layer should be $5e14cm^{-3}$ to $5e17cm^{-3}$, and the thickness should be 0.05 μm to 1.5 μm.



Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) Set: Hyung Ryu		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

6. pattern n epilayer

Selectively remove n- epilayer on top of contacts and in the field area either by RIE (or other dry etch techniques or sacrificial oxidations)

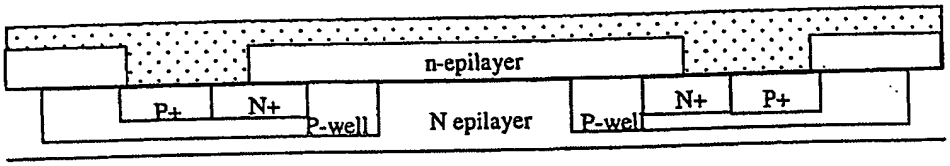


N- drift region

N+ Substrate

7. Gate dielectric formation

After the implant activation, a suitable gate dielectric material is deposited or grown on top of the structure.



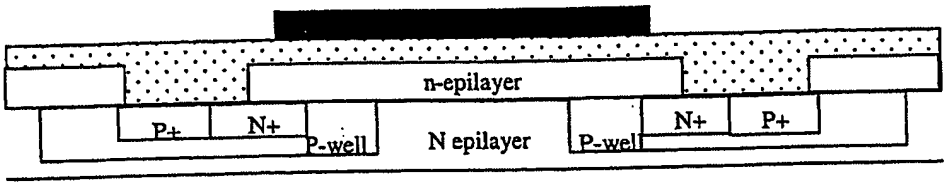
N- drift region

N+ Substrate

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1)		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

10. Gate metal deposition

Gate metal is deposited then patterned to form gate electrodes. Metals such as Molybdenum or polysilicon can be used at this step.

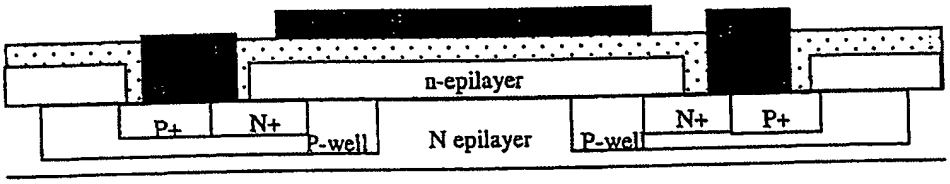


N- drift region

N+ Substrate

11. Formation of Contacts

Contact windows are open in the dielectric layer and contact metal is deposited. Ni or Ti is typically used for N-type ohmic contacts and Ni, Ti, Pt, or Al is used for P-type ohmic contacts. After the metal deposition, the contacts are sintered in vacuum or in Argon at temperatures from 500°C to 1200°C, for a duration of 1 sec to 20 minutes.



N- drift region

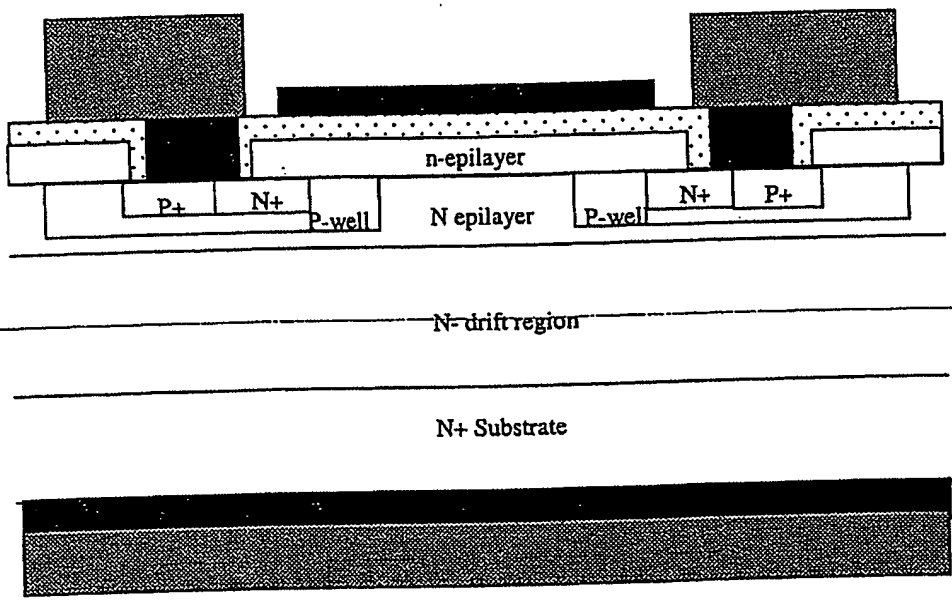
N+ Substrate

[redacted]

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1) [redacted]		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

12. Overlayer

Finally, overlayer metal is deposited and the fabrication is complete.



Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1)		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

Advantage:

The suggest structure increase the on-current significantly using the conventional processing technology and without sacrificing the blocking voltage.

Disadvantage:

The starting epi structure is slightly more complicated than the one for conventional structure.

Applications.

High power switching

High frequency (~ 1MHz) power switching.

Motor control.

Inventor's Full Signature	Date	Witnessed, read and understood:	Date
(1)		(1) Anant Agarwal	
(2)		(2)	
(3)		(3)	

4600 Silicon Drive • Durham, NC 27703 • (919) 313-5300 • (919) 313-5452 FAX

December 16, 2002

VIA FEDERAL EXPRESS

Timothy J. O'Sullivan, Esq.
Myers Bigel Sibley & Sajovec, P.A.
4140 Parklake Avenue, Suite 600
Raleigh, NC 27612

Re: New U.S. Provisional Application entitled *A Novel Planar Power MOSFET Transistor in Silicon Carbide with Vertical JFET Limiter to Reduced JFET Resistance and a Method of Fabrication*
Our Ref.: P0279

Dear Tim:

Please proceed to prepare and file a U.S. provisional application for the invention described in the enclosed invention disclosure. If you have any questions about the disclosure, please do not hesitate to contact the inventor, Sei-Hyung Ryu, directly. **Please file this application as soon as possible.**

Please send carbon copies of all drafts and correspondence for this case to my attention.

Thank you for your attention to this matter. If you have any questions, please do not hesitate to contact me.

Very truly yours,

David C. Hall
Associate General Counsel
Intellectual Property

Enclosures
MCS-B093

B

MYERS BIGEL SIBLEY & SAJOVEC, P.A.

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Richard P. Vitek

December 19, 2002

Via Hand Delivery

Sei-Hyung Ryu
Cree, Inc.
4600 Silicon Drive
Durham, North Carolina 27703

Re: *Vertical Jfet Limited Silicon Carbide Power Metal-Oxide Semiconductor Field Effect Transistors And Methods Of Fabricating Vertical Jfet Limited Silicon Carbide Metal-Oxide Semiconductor Field Effect Transistors*
Cree Docket No.: P0247; Our File: 5308-247PR

Dear Sei-Hyung:

Attached please find a working draft of the above-referenced provisional patent application for your review.

It is essential that the patent application, as filed, be technically accurate and complete, and sets forth the best mode of carrying out your invention. Since new matter may not be added to the descriptive portion after filing, we ask that you, carefully review the draft for technical accuracy and completeness, and advise us of any suggested changes or corrections. Your changes and suggestions will be carefully considered in the preparation of the final draft.

Out of an abundance of caution, we are requesting that you confirm that the proper inventive entity has been identified for the claimed invention(s). At present, you have been identified as the only inventor. As you may be aware, inventorship is determined based upon the subject matter of the claimed invention. Generally stated, to be an inventor one must have made an actual contribution to the conception of the operative invention which is claimed. There may be joint inventorship even though the joint inventors (a) did not work physically together or at the same time, (b) did not make an equal contribution or (c) did not make a contribution to the subject matter of every claim of the patent. A worker who merely carries out the instructions of another or only provides implementing devices to carry out another's ideas where the effort to do so is the exercise of one of ordinary skill is not typically an inventor. Further, all persons listed as co-authors on an article describing or related to the invention are not necessarily inventors. Please feel free to call with any questions you may have on this issue. There is no need to respond on this matter if the inventorship is correct.

We would also like to point out that each inventor is required to make a Declaration when the application is filed in the U.S. Patent and Trademark Office, acknowledging a duty to disclose information of which he or she is aware and which may be considered to be material to the

examination of the application. "Material" in this respect is defined as information that an examiner would likely consider important in deciding whether to issue a patent.

"Material" information as defined above may possibly include devices, products, publications, etc. which are similar to your invention and which were publicly known before your invention, and it may also include any public disclosure commercial use, or offer of sale of your invention more than one year prior to the filing date of your application.

If you are aware of any information (or subsequently become aware of information) which you believe might be considered "material", it is vitally important that it be brought to our attention. We can then make a determination as to whether the information should be brought to the attention of the Patent and Trademark Office under the applicable rules. Please also be aware that the duty to disclose information continues throughout pendency of the application, until the application issues as a patent. The duty to disclose information continues throughout the pendency of the application until a patent actually issues.

You should also be aware that certain activities either in the United States or foreign countries prior to filing of the application in the United States may have a bearing on your ability to file corresponding applications in foreign countries under the applicable international treaty. These activities could include public disclosure of your invention in either written or oral form, such as published articles, theses, patents, product announcements and proposals as well as through commercial exploitation of your invention, including public demonstrations, offers to sell, and sale of products incorpora ting your invention.

If you would like to preserve your right to file corresponding foreign applications on this invention, we recommend that all such activities should be avoided until the U.S. application is on file.

Please let us have your comments as soon as possible. If you should have any questions, please feel free to give me a call.

Best regards.

Sincerely,

Timothy J. O'Sullivan

TJO/tb
Enclosures
cc: David C. Hall, Esq. (w/ enc.)

MYERS BIGEL SIBLEY & SAJOVEC, P.A.

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December 20, 2002

David C. Hall, Esq.
Cree, Inc.
4600 Silicon Drive
Durham, North Carolina 27703

RE: *Vertical Jfet Limited Silicon Carbide Power Metal-Oxide Semiconductor Field Effect Transistors And Methods Of Fabricating Vertical Jfet Limited Silicon Carbide Metal-Oxide Semiconductor Field Effect Transistors*
Cree Docket No.: P0247; Our File: 5308-247PR

Dear David:

The above-referenced provisional patent application was filed in the United States Patent and Trademark Office by the express mail procedure on December 20, 2002 and should receive this date as the official filing date. We have enclosed a copy of this application and the accompanying documents as filed for your records. We also have enclosed a diskette containing the application in Microsoft Word format.

We will keep you advised of correspondence from the Patent Office regarding this application.

Best regards.

Sincerely,

Timothy J. O'Sullivan

TJO/tb
Enclosures

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D